BUMPLESS FLIP CHIP ASSEMBLY WITH SOLDER VIA

The present application is an application filed in accordance with 35 U.S.C. §119 and claims the benefit of earlier filed Singapore application number 9804817-6 filed on 17 December 1998.

1. Field of the Invention

This invention relates generally to a semiconductor device assembly, and in particular, relates to a connection of the integrated circuit (IC) chip or chips to a substrate circuitry, printed circuit board, and interconnect components. More specifically, the present invention relates to a chip assembly that includes a single or multi-layered substrate of which circuitry is connected to the input/output terminal pads of the IC chip through solder reflow in the via apertures or holes. The solder deposition techniques include electrolytic plating, electroless (chemical) plating, wave soldering, meniscus coating and solder printing techniques.

2. Background of the Invention

Recent developments of semiconductor packaging suggest an increasingly critical role of the technology. New demands are coming from requirements for more leads per chip and hence smaller input/output terminal pitch, shrinking die and package footprint, higher operational frequency that generate more heat, thus requiring advanced heat dissipation designs. All of these considerations must be met and, as usual, placed in addition to the cost that packaging adds to the overall semiconductor manufacturing costs.

Conventionally, there are three predominant chip-level connection technologies in use for integrated circuits, namely wire bonding, tape automated bonding (TAB) and flip chip (FC) to electrically or mechanically connect integrated circuits to leadframe or substrate circuitry. Wire bonding has been the far most broadly applied technique in semiconductor industry because of its maturity and cost effectiveness. However, this process can be performed only one at a time between semiconductor chip's bonding pads and the appropriate interconnect points. Furthermore, because of the ever increasing operational frequency of the device, the length of the interconnects need to be shorter to minimize inductive noise in power and ground, and also to minimize crosstalk between the signal leads. An example of such a method is disclosed in U.S. Pat. No. 5,397,921 issued to Kamezos et al.

Flip chip technology is characterized by mounting of the unpackaged semiconductor chip with the active side facing down to a interconnect substrate through some kind of contact anchors such as solder, gold or organic conductive adhesive bumps. The major advantage of flip chip technology is the short interconnects which can, therefore, handle high speed or high frequency signals. There are essentially no parasitic elements, such as inductance. Not only is the signal propagation delay slashed, but much of the waveform distortion is also eliminated. Flip Chip also allows an array interconnecting layout that provides more I/O than a perimeter interconnect with the same die size. Furthermore, it requires minimal mounting area and weight which results in overall cost saving since no extra packaging and less circuit board space is used. An example of such a method is disclosed in U.S. Pat. No. 5,261,593 issued to Casson et al.

While flip chip technology has tremendous advantage over wire bonding, its cost and technical limitations are significant. First of all, prior art flip chip technology must confront the challenges of having to form protruded contact anchors or bumps to serve as electrical connections between integrated circuit chip and substrate circuitry. Examples of such an approach are disclosed in U.S. Pat. No. 5,803,340 issued to Yeh, al. et. al. and U.S. Pat. No. 5,736,456 issued to Akram. These approaches typically include a very costly vacuum process to deposit intermediate under-bump layer that serves as adhesive and diffusion barrier. This barrier layer is typically composed of a film stack that can be in the structure of chromium/copper/gold. Bumping materials such as solder are subsequently deposited onto this intermediate layer through evaporation, sputtering, electroplating, solder jetting or paste printing methods followed by a reflow step to form the solder contacts. Although evaporation and sputtering techniques can potentially offer high density bumps, these processes need very tight control and normally result in poor yield. As a result, a conventional flip chip assembly is not only very costly but also suffers from very serious reliability concerns and high fatality ratio.

Techniques for fabricating the intermediate under-bump barrier layer as well as bump material utilizing electroless plating methods are also in the prior art. An example of such a method is described in the U.S. Pat. No. 5,583,073 issued to Lin et al. Although the electroless technique provides an economical, simple and effective method for providing an under-bump barrier layer, contacting material such as solder or adhesive is

still required for assembling. Solder dipping or screen printing of solder paste onto these bumps has been explored but has been met with very limited success due to lack of solder bridging control and non-uniform deposition of solder on the metal bump. This process can be very troublesome and suffers from poor process control as input/output terminal pad space is getting closer and closer together.

In view of the limitations of currently available integrated circuit assembling methods, a high performance, reliable and economical device and method that can effectively interconnect integrated circuits to the external circuitry would be greatly desirable.

SUMMARY OF THE INVENTION

It is therefore, an object of the present invention to provide a flip chip assembly to address high density, low cost and high performance requirements of semiconductor packaging. The device and method of the present invention involves the bonding of substrate circuitry to semiconductor device through the reflowing of pre-deposited solder to connect via apertures or holes of the substrate to terminal pad of the semiconductor device without the need for conventional bump, bonding wire, or other media.

To achieve the foregoing, the assembly includes a rigid or flexible dielectric substrate having a plurality of electrically conductive circuitry and a plurality of via apertures or holes. The conductive traces on the surface of the substrate are extended into each specific via hole through the conductive material deposited thereon. This through-hole (PTH) material such as plated copper provides a conductive base for solder deposition or solder wetting. Soldering material such as tin-lead alloy or lead-free solder is pre-deposited in the via hole or on the terminal pad. This readily available solder is to serve as the joint material after the substrate is attached to the semiconductor chip. The orientation of the attachment between chip and substrate circuitry ensures that at least one of the via holes in the dielectric substrate are aligned on the top of the terminal pad.

After alignment, the IC chip is brought in contact with the dielectric substrate through adhesive film or paste, or mechanical techniques. This soft or proximity contact is to ensure that the pre-deposited soldering material is able to reflow into the via hole as well as onto the terminal pad when it is molten. Heat, which serves to activate the flux and bring the solder to

its melting point, is used to effect the metallurgical bonding. This re-flow process results in a solder joint which will electrically and physically connect the via hole and IC pad fro permanent contact thereafter. This is important in that it not only assures a very cost effective and simple process, but also provides a compliant joint with significant stress release which results in a very reliable connection between the substrate circuitry and IC chip.

In one embodiment of the invention, the solder pre-deposition is in the via hole. In this embodiment, the via holes are first metallized with a base metal by conventional plated through hole (PTH) technique followed by the various solder deposition techniques. These include electroplating, wave soldering, meniscus solder coating, solder paste printing and dispensing techniques to accomplish the said pre-coating of solder materials onto the metallized hole wall. It is understood from the teaching herein that the particular solder or solder paste and methods of dispensing techniques depicted here is not meant to limit the invention.

In another embodiment of the invention, the solder pre-deposition is on the IC terminal pad. In this method, a barrier layer over-coated on the aluminum pad before solder deposition is preferred. This is to provide a good solder wetting surface and protect the aluminum surface against leaching, oxidation or degradation resulting from heat and soldering contact. This coating can be accomplished by sputtering a stake of thin film or by wet chemical direct plating of electroless nickel and immersion gold. For copper terminal pads, the pre-treatment may not be necessary when its surface is free of oxide and contamination.

The via holes of the substrate circuitry can be formed by various techniques including mechanical drilling, punching, plasma etching or laser drilling. They are formed in the substrate before or after the circuitry patterning depends on the various fabrication processes. The via holes are formed at locations where electrical circuitry on one side of the substrate can be connected to the opposite side of the surface on which the semiconductor chip or chips are mounted and their input/output terminal pads can be aligned thereon.

A preferred application of heat to reflow pre-deposited solder is by convection oven. Alternatively, the heat may be applied by laser to effect solder reflow and bonding to the IC terminals which are in the vicinity of the via holes. Another example of such an approach is an infrared (IR) continuous belt reflow oven. Alternatively, hot nitrogen gas may be directed onto the solder members of the assembly.

In summary, using soldering material directly reflowed between via hole and terminal pad can effectively connect IC chip and dielectric substrate circuitry without external bumps or wires. This approach allows a reliable, low profile, high performance and low cost assembly to be achieved. In particular, a small via hole which can be formed by laser or other techniques allows very fine pitch terminal pad to be interconnected, can significantly enhance the capability of packaging future high I/O semiconductor chips.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a fragmented partial sectional side elevational view of a substrate before plating the via hole with solder.

Figure 1B is a fragmented partial sectional side elevational view of the substrate of the type shown in Figure 1A after plating the via hole with solder.

Figure 1C is a fragmented partial sectional side elevational view of a die having a terminal pad.

Figure 1D is a fragmented partial sectional side elevational view of a chip assembly after a die of the type shown in Figure 1C has been attached to a substrate of the type shown in Figure 1B.

Figure 1E is a fragmented partial sectional side elevational view of the chip assembly of the type shown in Figure 1D after a solder reflow process.

DETAILED DESCRIPTION OF THE INVENTION

The bumpless flip chip assembly of the present invention includes a rigid or flexible dielectric substrate having a plurality of electrically conductive circuitry and a plurality of via apertures or holes. The conductive traces on the surface of the substrate are extended into each specific via hole through the conductive material deposited thereon. This through-hole (PTH) material such as plated copper provides a conductive base for solder deposition or solder wetting. Soldering material such as tin-lead alloy or lead-free solder is pre-deposited in the via hole or on the terminal pad. This readily available solder serves as the joint material after the substrate is attached to the semiconductor chip. The orientation of the attachment between chip and substrate circuitry ensures that at least one of the via holes in the dielectric substrate are aligned with a terminal pad.

After alignment, the IC chip is brought in contact with the dielectric substrate through adhesive film or paste, or mechanical techniques. This soft or proximity contact is to ensure

that the pre-deposited soldering material is able to reflow into the via hole as well as onto the terminal pad when it is molten. Heat, which serves to activate the flux and bring the solder to its melting point, is used to effect the metallurgical bonding. This re-flow process will result in a solder joint which will electrically and physically connect the via hole and IC pad for permanent contact thereafter. This is important in that it not only assures a very cost effective and simple process, but also provides a compliant joint with significant stress release which results in a very reliable connection between the substrate circuitry and IC chip.

As defined herein, the preferred embodiment is particularly directed to the bonding of an integrated circuit (IC) chip to a flexible circuitized substrate, or to a more rigid, circuitized substrate, a particular example of the later being a printed circuit board. It is to be understood, however, that the invention is not limited to the attachment to printed circuit boards, in that other circuitized substrates, including known ceramic substrates, may be employed. Typically, organic-type substrate is preferable for the purpose of lower cost, superior dielectric property whereas inorganic-type of substrate is preferable when high thermal dissipation and matched coefficient of expansion are desired. By the term "substrate" as used herein is defined as at least one layer of dielectric material having at least one conductive layer thereon. Printed circuit boards of similar type are well known in the electronics industry, as well as the processes for making the same, and therefore, further definition is not believed to be necessary. Such structures may include many more electrically conductive layers than those depicted in FIGS 1A through 1E, depending on the desired operational characteristics. As is known, such electrically conductive layers may function as signal, power, and/or ground layers.

In one embodiment of the invention, the solder pre-deposition is in the via hole. In this embodiment, the via holes are first metallized with a base metal by conventional plated through hole (PTH) technique followed by the various solder deposition techniques. These include electroplating, wave soldering, meniscus solder coating, solder paste printing and dispensing techniques to accomplish the said pre-coating of solder materials onto the metallized hole wall. It is understood from the teaching herein that the particular solder or solder paste and methods of dispensing techniques depicted here is not meant to limit the invention.

In another embodiment of the invention, the solder pre-deposition is on the IC terminal

pad. In this method, a barrier layer over-coated on the aluminum pad before solder deposition is preferred. This is to provide a good solder wetting surface and protect the aluminum surface against leaching, oxidation or degradation resulting from heat and soldering contact. This coating can be accomplished by sputtering a stake of thin film or by wet chemical direct plating of electroless nickel and immersion gold. For copper terminal pads, the pre-treatment may not be necessary when its surface is free of oxide and contamination.

The via holes of the substrate circuitry can be formed by various techniques including mechanical drilling punching, plasma etching or laser drilling. They are formed in the substrate before or after the circuitry patterning depends on the various fabrication processes. The via holes are formed at locations where electrical circuitry on one side of the substrate can be connected to the opposite side of the surface on which the semiconductor chip or chips are mounted and their input/output terminal pads can be aligned thereon.

A preferred application of heat to reflow pre-deposited solder is by convection oven. Alternatively, the heat may be applied by laser to effect solder reflow and bonding to the IC terminals which are in the vicinity of the via holes. Another example of such an approach is an infrared (IR) continuous belt reflow oven. Alternatively, hot nitrogen gas may be directed onto the solder members of the assembly. It is understood from the teaching herein that the particular re-flow techniques depicted above is not meant to limit the invention, in that it is also possible to reflow the solder by vapor phase reflow system.

If the finished product is, for instance, a ball grid array package, solder balls will normally be placed on the specific pads on the surface of the dielectric substrate. This finished package can be connected to a printed circuit board by reflowing the solder balls to form an attachment to the traces of the printed circuit board.

FIGS. 1A to 1E are diagrammatic cross-sectional views showing steps involved in the manufacturing of an integrated circuit assembly by pre-depositing solder in the substrate via hole and re-flowing to connect the terminal pad.

Referring initially to FIG 1A, a substrate 101 having a plurality of electrically conductive circuitry traces 102 partially covered by the solder mask 103 is shown. The traces 102 on the substrate extend into a plurality of via holes 104 by a thin layer of plated through-hole copper 105 deposited thereon.

FIG. 1B shows the substrate is immersed in a solder plating solution and a layer of

solder 106 is electroplated on the metallized via hole wall as well as on the solder opening site.

FIG. 1C shows an integrated circuit chip 107 having various types of transistor, wires and the like (not shown), which has a plurality of exposed input/output terminal pads 108. These pads 108 were deposited with a stake of thin film 109 in the structure of titanium (500 Angstroms)/nickel (700 Angstroms)/gold (1000 Angstroms) to serve as the barrier and adhesive layer.

FIG. 1D shows IC chip 107 securely attached to the substrate circuitry 101 by adhesive paste ABLESTIK "ABLEBOND 961-2" 110 to form an assembly 111. The orientation of the attachment is arranged in such a manner that the specific terminal pad 108 of the integrated circuit chip 107 is in contact with a specific via hole 104. The via hole 104 is to serve as the electrically connecting channels for respective traces 102 of the substrate 101.

FIG. 1E shows the input/output terminal pad 108 firmly joined together with a specific via hole 104 to become an integral part after the assembly 111 was placed in an oven for a solder reflow. This simultaneously-reflowed joint 112 provides an effective means for electrical and mechanical connections between IC chip 107 and the dielectric circuitry 101. The soldering material 113 deposited in the solder mask opening serves as the contacting material for the next level assembly.

Though only one integrated circuit chip 107 is shown in the figure, it is to be understood that additional integrated circuit chips, as well as passive components such as resistors or capacitors, can also be mounted on the substrate circuitry 101.

Though only one solder system is shown in the figure, it is to be understood that many solder systems including lead-free ones, can also be applied and serve the connection purpose.

The present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The presently disclosed embodiments are, therefore, to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are, therefore, to be embraced therein.

What is claimed is: